Abstract of the Disclosure

The current cell matrix includes 63 upper current cells and one lower current cell. Each of the current cells has 4 constant current transistors having the same size with respect to each other. The upper current cell outputs drain currents of all the constant current transistors when the cell is selected by the upper decoder. The lower current cell outputs drain currents of none, one or two constant current transistors in accordance with the select signal from the lower decoder. The analog output terminal combines and outputs the currents of the selected constant current cells. The current cell type digital-to-analog converter has the decreased differential linearity error and the decreased integral linearity error.